EE 648
VLSI Design

COURSE INFORMATION

Instructor: Dr. Jason McNeely, Duckering 227
Office Phone: 474-7228
Email: jbmcneely@alaska.edu
Office Hours: Monday 2:00-4:00; Thursday 2:30-4:30
(You may also schedule an appointment or just drop by. The best way to reach me outside of office hours is via email.)

Lectures: MWF 10:30-11:30
Location: DUCK 406

Credits: 3

Prerequisites: EE 343 or equivalent

Textbook: *CMOS VLSI Design: A Circuits and Systems Perspective* 4th Edition, Neil Weste and David Harris. 2011 Pearson Education. ISBN 978-0-321-54774-3

References: Other reference materials may be posted electronically during this course.

Methodology: Lectures will be supplemented with relevant homework including use of CAD tools and projects that combine theory with practical design. Quizzes and exams will assess the theoretical components, while projects with a brief presentation will assess the practical skills. Blackboard will be used for electronic material posting.

COURSE DESCRIPTION

This course will cover the skills necessary to bring a basic digital design having many transistors from concept to custom or semi-custom chip design for fabrication. This complements the computer engineering curriculum by allowing the student to move from the FPGA based and embedded system based design background to full custom chips. The design flow from concept all the way to final layout product will be emphasized. These are some of the skills needed by engineers at semiconductor companies. Hands on experience with some basic layout tools will be assigned via projects.

Students enrolling in this course need to have at least one semester of digital logic design (EE 343 or equivalent). It is also helpful to have some electronics background as well.

The catalog course description:
Study of methods to integrate millions of transistors on a single chip and create optimized designs. Topics include CMOS logic design, power and timing issues, VLSI architectures, and full custom layout. Students will use CAD tools to implement a VLSI design

COURSE GOALS/OUTCOMES

Students taking this course will be able to:

- Design CMOS circuits at the transistor level and use CAD tools to create the chip
- Start with a design concept at a transistor level or schematic and produce a layout
- Understand the industry standard methods of logic design and layout

Student learning outcomes would be the ability to:

- Design full custom IC VLSI design using the MAGIC CAD tool
- Design logic circuits using CMOS transistor family
- Comprehend performance issues in CMOS circuits such as power and delay
- Have an ability to create dynamic CMOS designs
- Simulate, verify, and analyze the performance of layouts

IMPORTANT DATES

Thursday January 17:	First day of classes
Monday January 21:	Alaska Civil Rights Day (no classes)
Friday February 1:	Last day to drop the class (course does not appear on academic record)
March 11-15:	Spring break (no classes)
Friday March 22:	Last day to withdraw ('W' appears on academic record)
Friday April 26:	UAF SpringFest (no classes)
Monday May 6:	Last day of class
Tuesday-Friday May 7-10:	FINAL EXAMS
May 8 10:15-12:15	**FINAL EXAM for VLSI**

(Dates from 2013. Will be changed in 2015)

(Dates on schedule below are from 2013. Will be changed in 2015)

L	Date	Topic(s)	Book Sections	Homework/Quizzes
1	Friday 1/18	History and Review of CMOS configuration	1.1-1.3	
Monday January 21: Alaska Civil Rights Day				
2	Wednesday 1/23	Static CMOS Layout Rules/Gates	1.4-1.5 Skip 1.4.9	HW #1: 1.1, 1.6, 1.8. Tristate Drawing Install MAGIC
3	Friday 1/25	Circuit Fabrication MAGIC Layout Tool tutorial	1.5 MAGIC Intro	
4	Monday 1/28	Finish Tutorial Semicustom Design Flow	1.9	HW #2: Work through MAGIC tutorials 1-3 Draw and turn in series nMOS in MAGIC
5	Wednesday 1/30	Delay/Power Intro Transistor Operating Regions	1.9 2.1-2.2	**Quiz 1**
6	Friday 2/1	MOS Operating Regions+Current	2.1-2.2	HW #3: 2.1 and custom problem
7	Monday 2/4	Simple MOS Capacitance Nonideal IV	2.3-2.4	HW #4: Research
8	Wednesday 2/6	DC Transfer Curve Noise Margins	2.5	HW #5: 2.14, 2.15 Install ng-spice
9	Friday 2/8	CMOS Process Technologies Fabrication	3.1-3.2	
10	Monday 2/11	Layout Design Rules	3.3	HW #6: Inverter Layout in MAGIC; Simulate DC transfer
11	Wednesday 2/13	Process Enhancements	3.4	
12	Friday 2/15	Circuit Simulation SPICE	8.1	
13	Monday 2/18	SPICE Subcircuits ; Models; Delay	8.2.4-8.3	
14	Wednesday 2/20	Simulation Pitfalls How to Determine Delay Part I	End of 8 4.1-4.2	HW #7: Go back to Inverter layout and find delays
15	Friday 2/22	RC Model of Delay Elmore Delay	4.3	
16	Monday 2/25	The RC Model cont'd More examples; Inching toward linear delay model	4.3	

L	Date	Topic(s)	Book Sections	Homework/Quizzes
17	Wednesday 2/27	Finish RC Model; Linear Delay Model; Logical Effort	4.4	**Quiz 2**
18	Friday 3/1	Minimum Delay (Using path effort and then sizing path)	4.5	
19	Monday 3/4	Best number of stages	4.5	HW #8: 4.1,4.5,4.11; **Project Part I:Optimal Sizing in Magic for a Full Adder Carry Out**
20	Wednesday 3/6	Introduction and Types of Power in CMOS	5.1	
20b	Friday 3/8	EXAM I REVIEW		
Monday March 11 – Friday March 15: Spring Break				
	Monday 3/18	**EXAM I**		
21	Wednesday 3/20	Dynamic Power/Activity Factor	5.2	
22	Friday 3/22	Dynamic and Static Power	5.2-5.3	
23	Monday 3/25	Static Power Cont'd	5.3-5.4	HW #9: 5.2, 5.4, 5.7
24	Wednesday 3/27	Low power circuits; Intro to circuit families(Static CMOS)	5.5; 9.1	
25	Friday 3/29	Pseudo nMOS	9.2	**Project Part 2: Design sum circuit since carry out circuit is completed.**
26	Monday 4/1	CVSL; Dynamic Circuits	9.2	
27	Wednesday 4/3	Dynamic Cont'd; Domino and Dual Rail	9.2	
28	Friday 4/5	NP-Domino/Zipper Domino	9.2	**Quiz 3** HW#10: 9.3, 9.4, 9.1
29	Monday 4/8	Pass Transistors and Pitfalls	9.2-9.3	
30	Wednesday 4/10	Memory Systems; SRAM Cells	12.1-12.2	

L	Date	Topic(s)	Book Sections	Homework/Quizzes
31	Friday 4/12	SRAM Noise Margins	12.2	
32	Monday 4/15	SRAM Layout; Row/Col Circuits	12.2	
33	Wednesday 4/17	DRAM; ROM; FLASH	12.3+	
	Friday 4/19	**EXAM II**		
34	Monday 4/22	Introduction to Sequential Design	10.1-10.2.3	
35	Wednesday 4/24	Min time/Time borrowing/Clock Skew	10.2.3-10.2.5	
Friday April 26: UAF SpringFest – No Class				
36	Monday 4/29	Design of Latches	10.3.1	**Project Part 3: Design 8-bit Ripple Carry Adder/Subtracion**
37	Wednesday 5/1	Design of Flip Flops	10.3.2	
38	Friday 5/3	Sequencing/hold/setup/etc ; Addition circuits?	10.4.2; 11.1?	
39	Monday 5/6	Adders and Final Exam Review	11.1	

TENTATIVE SCHEDULE

42 Class Meetings = 37 Lectures + 1 Tutorial Day + 2 Exams + 2 Presentation days

FINAL EXAM: May 8 10:15-12:15

COURSE POLICIES

E-mail
Each student is expected to regularly check his or her **alaska.edu email address**. This address will be used for class correspondence - announcements, homework problems clarifications, etc. If you are not using the official UAF email address, please forward it to your address of choice.

Attendance
Class attendance is highly recommended. Material not in the text may be introduced at random intervals and occasional quizzes are part of your grade. If you miss a class, lecture slides and other handouts are available on Blackboard or can be obtained from the instructor. If you are late, please enter without disrupting the class.

Homework
Homework problems will typically be due the following class, unless otherwise stated. No late homework will be accepted without a valid excuse and prior arrangement.

You are expected to work independently (even if you work in study groups). The work you hand in should be your own effort. Any student whose work is copied from another student may receive a zero grade for the assignment. If you have questions about a homework problem outside of the instructor's or TA's office hours, please feel free to contact them by e-mail. Homework assignments are expected to be neat and legible. The grader is not obligated to decode scribbles; illegible answers will be assumed to be wrong.

Quizzes
You can expect to have a short quiz given every week, or even more frequently. Quizzes will typically cover the material from the previous week or two. The material for quizzes will include lectures, homework, reading assignments, and laboratory exercises. Unless otherwise stated, quizzes will be "**closed book**". Quizzes cannot be made up if missed.

Exams
There will be two exams and a final exam. No makeup exams will be given except for documented extenuating circumstances. If you can anticipate an absence (work commitments, intercollegiate sports), talk to your instructor before the exam to make arrangements. If the absence is unexpected (illness, family or personal difficulties), please inform your instructor at the earliest possible opportunity.

Custom Layout Project
A custom designed 8-bit adder will be required as the project for this course. Using the MAGIC VLSI layout tool, a static CMOS 8-bit adder will be designed, drawn, and simulated for functionality, area required on the chip, delay (the speed of the adder), and power consumption. Following completion of that part, the adder will be re-designed using a dynamic CMOS technology of your choice. Again, design and simulation will be completed. Finally, comparisons can be made between the two designs to aid in the understanding of the various pros and cons of the two technologies and will give insight as to why static CMOS is semiconductor industry's technology of choice even though dynamic logic has some advantages. If designs are completed early, it may be possible to even send some designs off for fabrication and get a chip back, although this will not be required.

STUDENTS WITH DISABILITIES

Students with learning or other disabilities who may need classroom accommodations are encouraged to make an appointment with the Office of Disability Services (208 WHIT, Phone # 474-5655). Please meet with me during office hours so that we can collaborate with the Office of Disability Services to provide the appropriate accommodations and supports to assist you in meeting the goals of the course.

GRADING

Grade Component	Percentage
Homework	15%
Quizzes	15%
Exams I and II	25%
Final Exam	25%
Project (in three stages)	20%

Grade	Final Score
A	>= 90%
B	>= 80%
C	>= 70%
D	>= 60%
F	< 60%

***Plus/Minus grading will be used.**

***** This scale is not absolute. Grades will be curved according to performance. However, the cutoff percentages listed here are maximum values such that a student with a final score of 90 will always receive an "A". In other words, the score required to achieve an "A" will never be set higher than 90%. The same applies to the other grade letters.

Projects will be graded based on completion, analysis, and brief presentation.

PLAGIARISM

As a UAF student, you are subject to UAF's Honor Code:
"Students will not collaborate on any quizzes, in-class exams, or take-home exams that will contribute to their grade in a course, unless permission is granted by the instructor of the course. Only those materials permitted by the instructor may be used to assist in quizzes and examinations.
Students will not represent the work of others as their own. A student will attribute the source of information not original with himself or herself (direct quotes or paraphrases) in compositions, theses and other reports. No work submitted for one course may be submitted for credit in another course without the explicit approval of both instructors.
Violations of the Honor Code will result in a failing grade for the assignment and, ordinarily, for the course in which the violation occurred. Moreover, violation of the Honor Code may result in suspension or expulsion."