3.4 Flight Computer

3.4.1 System Requirements

The general requirement for the flight computer is to manage all onboard-generated data, with reliable recovery of the data being the ultimate goal. Reliable recovery would be through transmission and/or nonvolatile memory (NVM) storage. (Figure 3.4.1.1) The required operation of the flight computer is outlined below.

3.4.1.1 Process incoming science and flight data analog signals (Figure 3.4.1.2)

- Switch analog muxes
- Direct ADC’s to sample and convert
- Direct ADC’s to release converted data
- Store data in RAM

3.4.1.2 Process incoming asynchronous GPS data (Figure 3.4.1.3)

- Detect and synchronize with incoming GPS data
- Store data in RAM

3.4.1.3 Time stamp incoming data

3.4.1.4 Format data into packets

3.4.1.5 Send packets to transmitter and memory (Figure 3.4.1.4)

- Science and flight data packets transmitted "on-the-fly"
- Science and flight data packets written to NVM in 512 byte blocks
- GPS data transmitted and at the same time stored in NVM

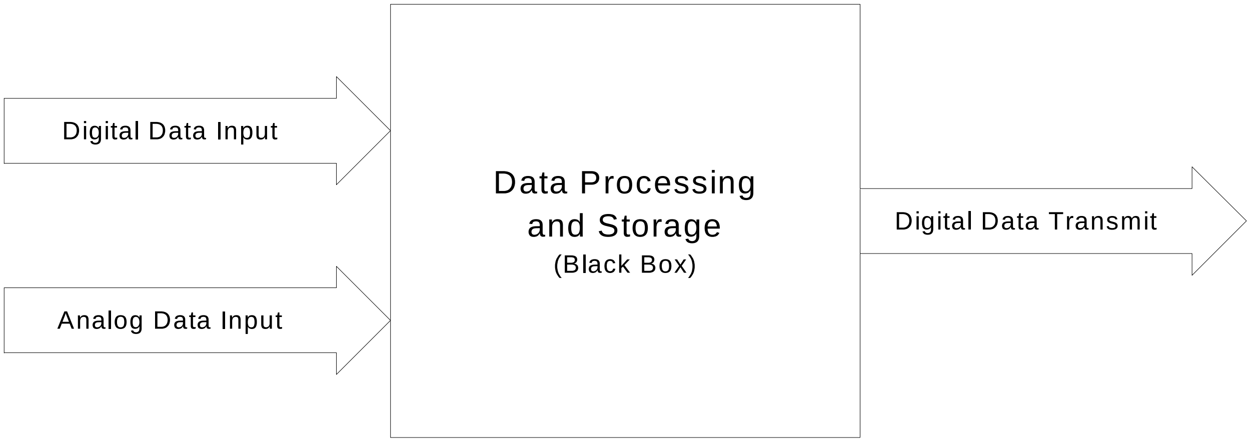

Figure 3.4.1.1: Flight Computer Black Box

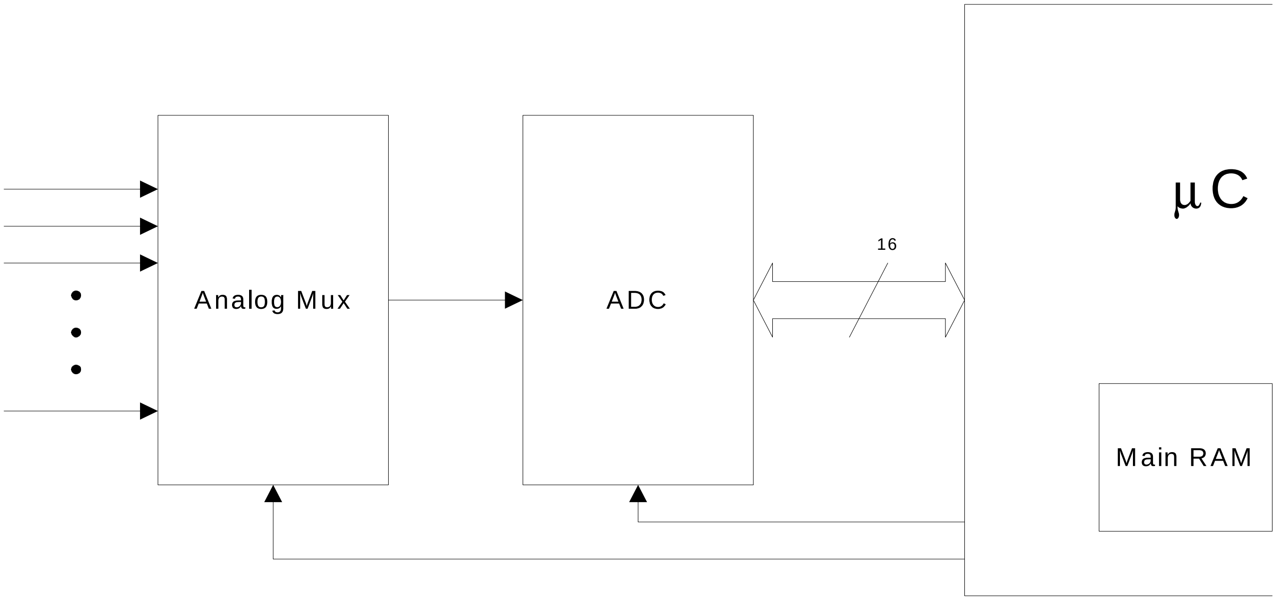

Figure 3.4.1.2: Processing of Analog Data

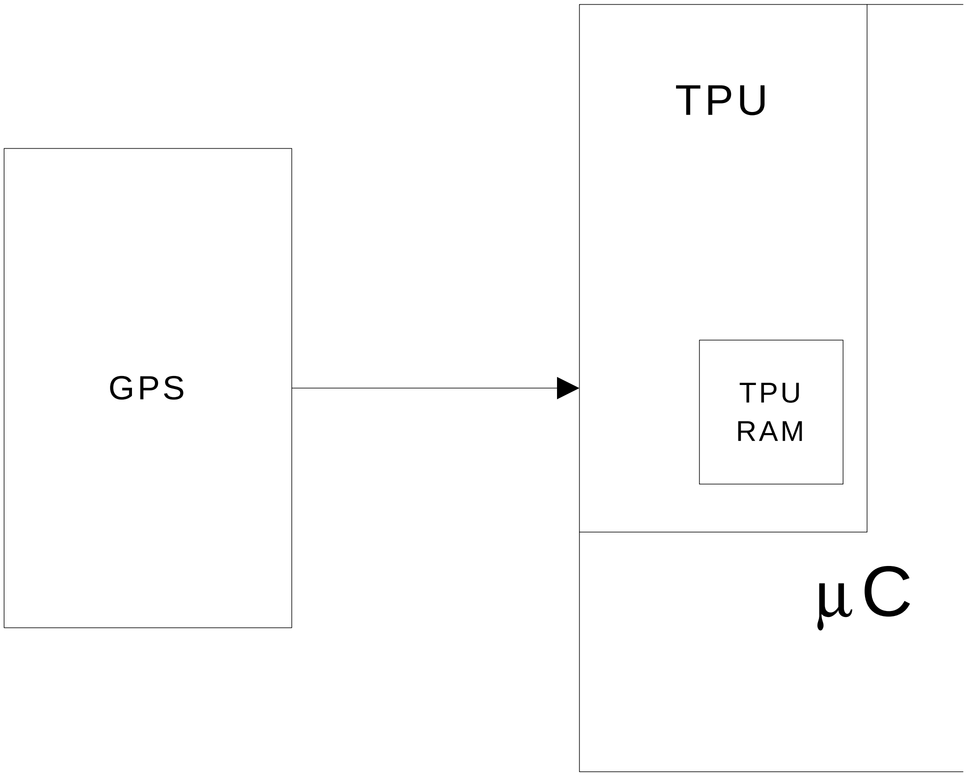

Figure 3.4.1.3: Processing of GPS Data

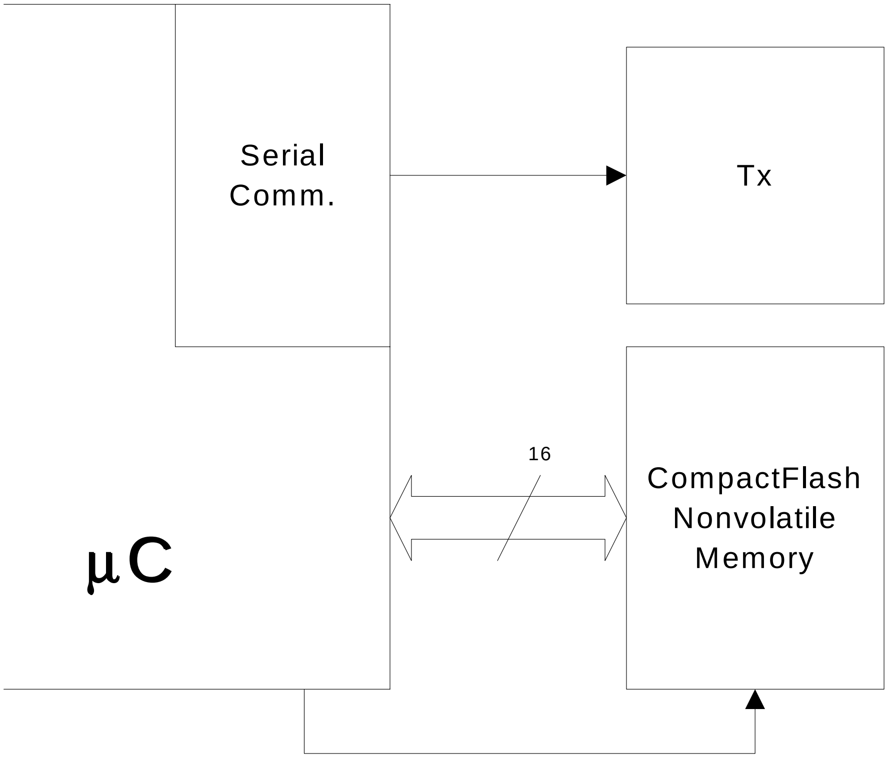

Figure 3.4.1.4: Transmission and Storage of Data

3.4.2 External Interfaces

The flight computer is broken up into two blocks, an analog-to-digital conversion (ADC) block, and a processing, storage, and communications (PSC) block. The ADC block's external interfaces are all incoming analog signals. All other inputs and outputs interface to the PSC block. The PSC block contains the microcontroller, which handles all the processing, the CompactFlash, which is used to store all data that comes through the microcontroller, the serial communications hardware, which handles driving serial communications between the microcontroller and an outside computer, and a latch, which handles all incoming status switch signals. Figure 3.4.2.1 shows all external interfaces to the flight computer and the interfaces are further detailed below.

3.4.2.1 Incoming Analog Signals

The ADC block is broken down into three sections, the 16-bit, -2.5 to +2.5 V section, the 16-bit, 0 to 5 V section, and the 12-bit, 0 to 5 V section. The three sections are named sixt2.5, sixt5, and twel5, respectively. Each section contains a different number of ADC component sets. Each set is composed of an analog multiplexer and an ADC. The only difference between sets from each section is a different ADC chip. The sixt2.5 section contains one ADC set with the ADC chip handling 16-bit conversion of -2.5 to +2.5 V input signals, with 8 channels available. The sixt5 section contains three ADC sets with the ADC chips handling 16-bit conversion of 0 to 5 V input signals, with 24 channels available. The twel5 section contains five ADC sets with the ADC chips handling 12-bit conversion of 0 to 5 V input signals, with 40 channels available. Table 3.4.2.1 summarizes this information. Figures 3.4.2.2 to 3.4.2.4 show the schematics for the ADC block.

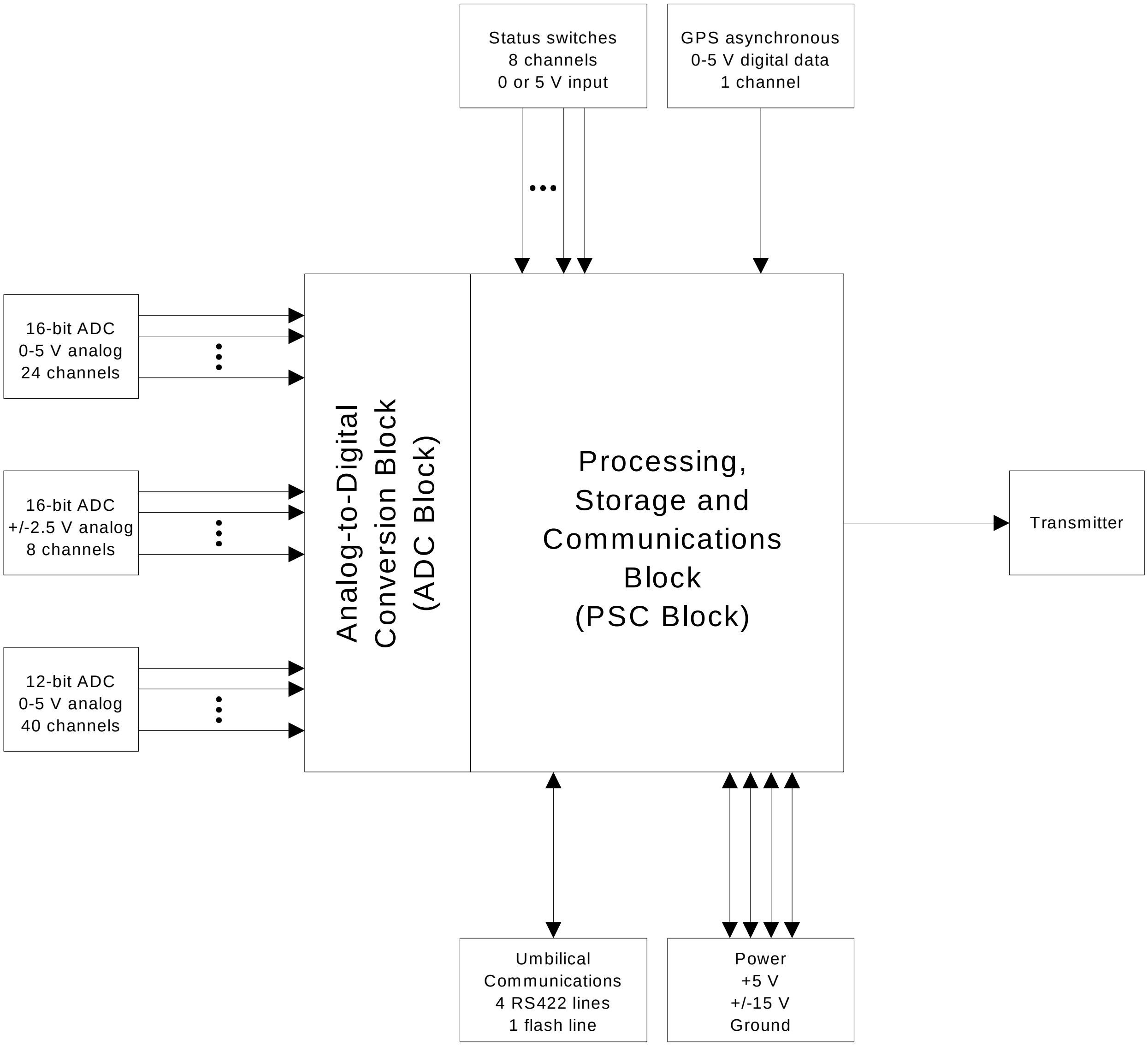

Figure 3.4.2.1: Flight Computer External Interfaces

Table 3.4.2.1: ADC Sections

Section Name	# of channels	Resolution	Input Voltage Range
sixt2.5	8	16-bit	-2.5 to +2.5 V
sixt5	24	16-bit	0 to 5 V
twel5	40	12-bit	0 to 5 V

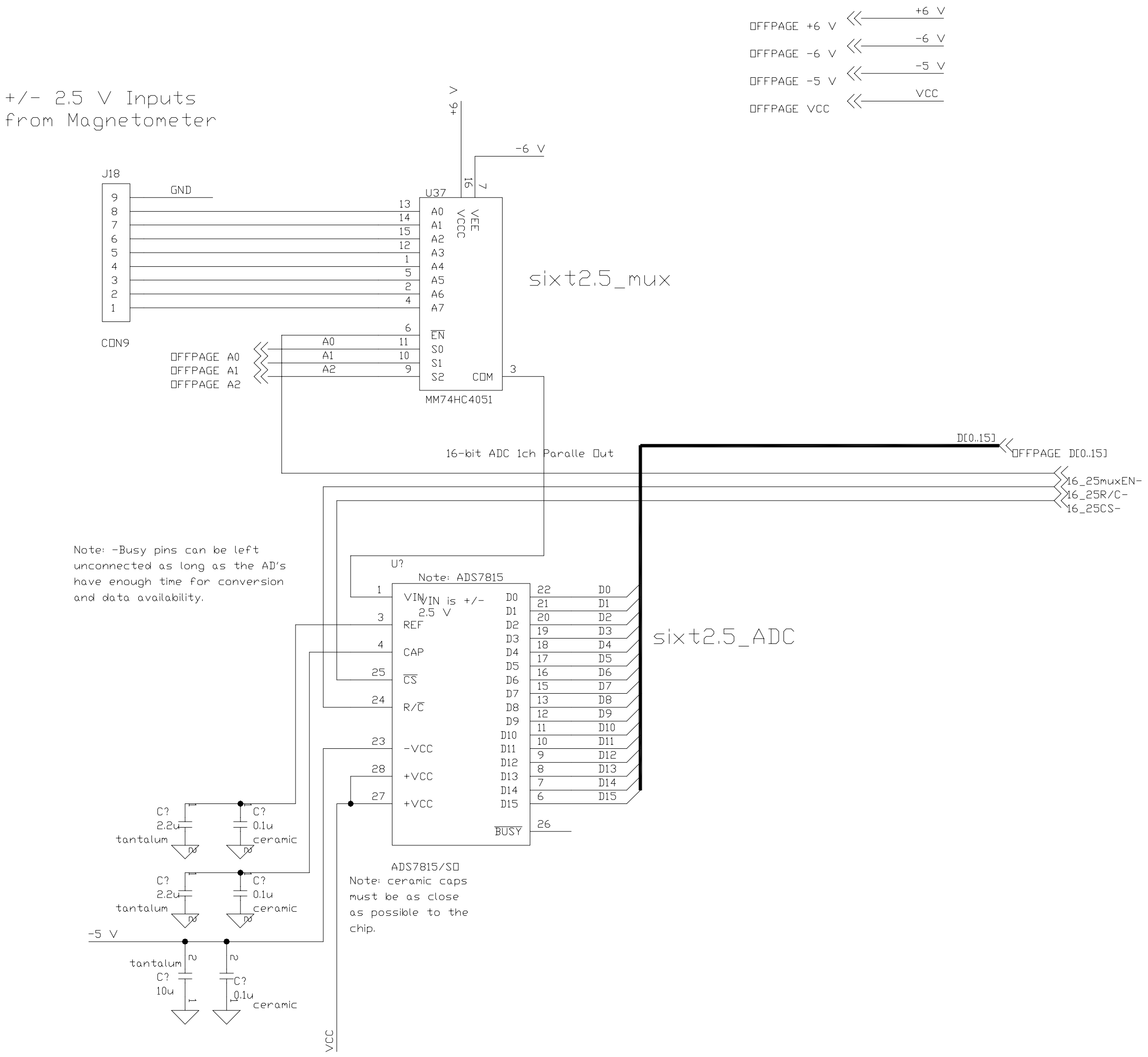

Figure 3.4.2.2: sixt2.5 ADC Section

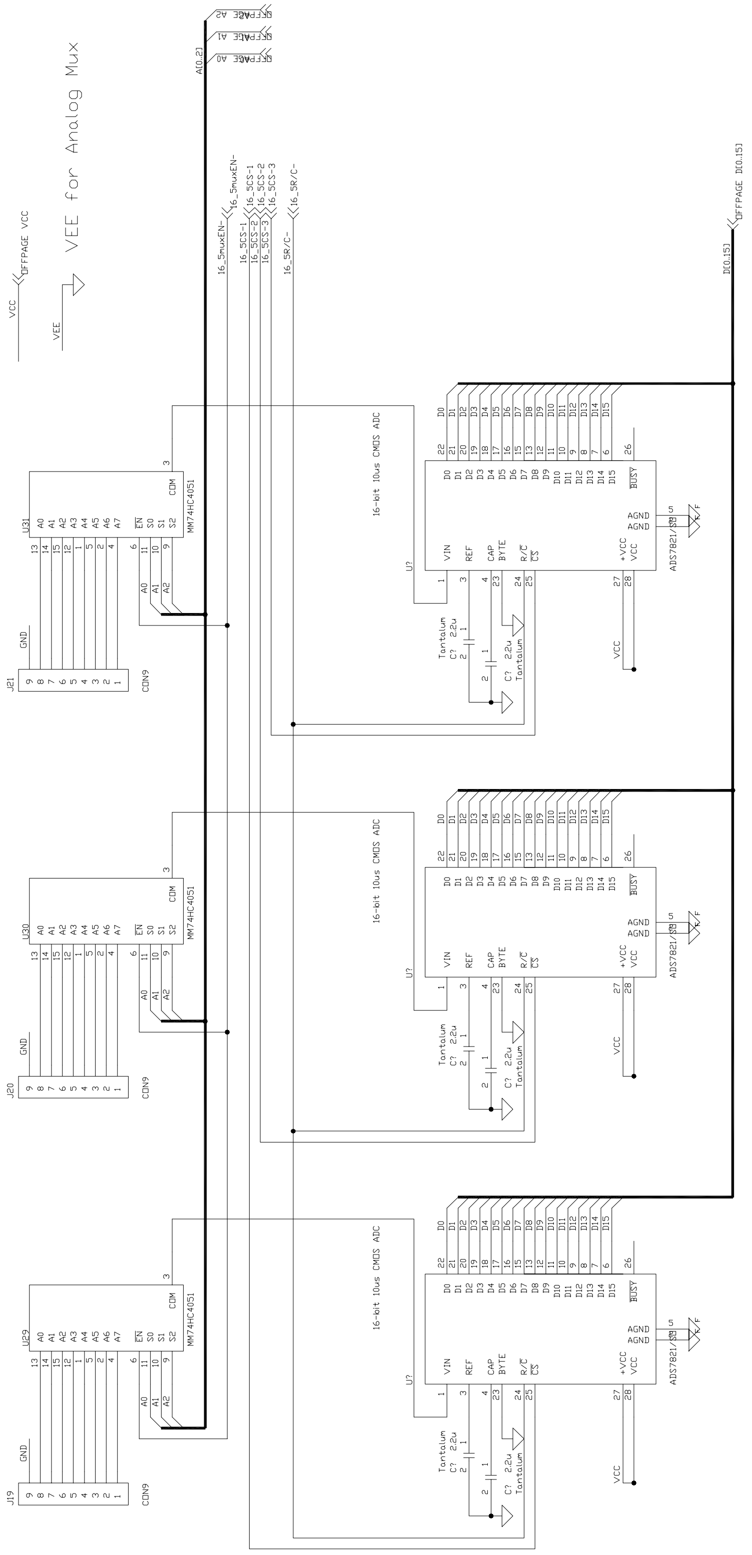

Figure 3.4.2.3: sixt5 ADC Section

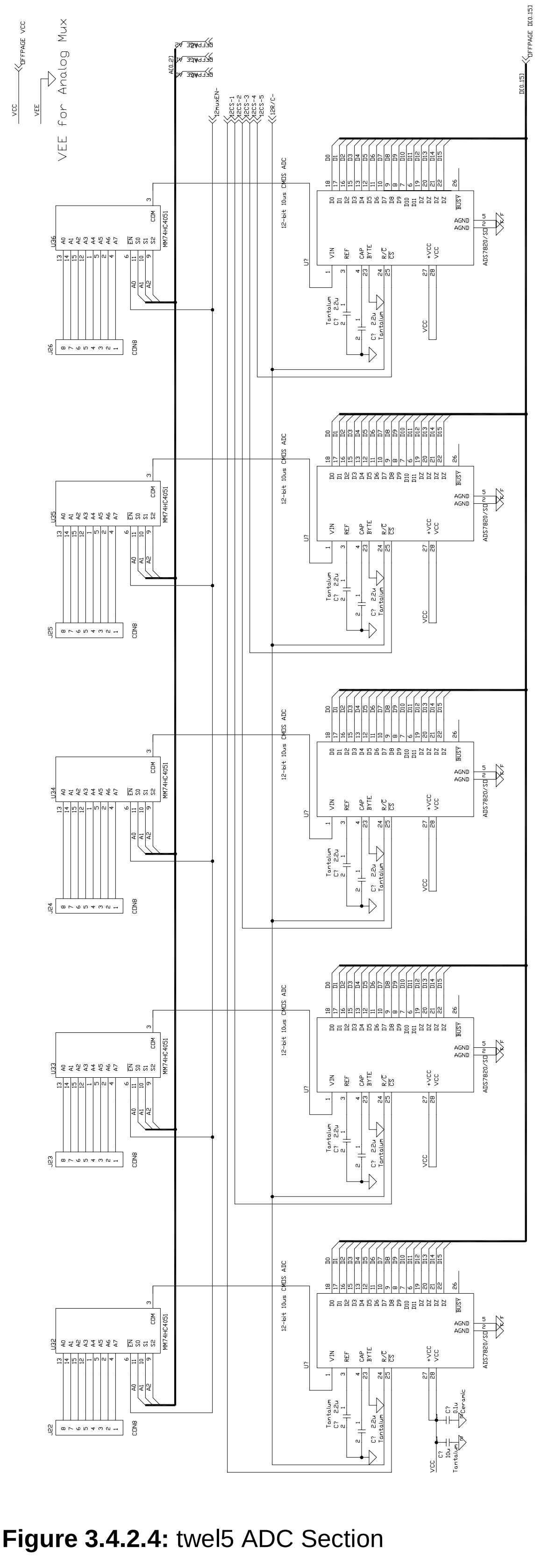

Figure 3.4.2.4: twel5 ADC Section

3.4.2.2 Incoming Digital Signals

Incoming digital data consists of asynchronous GPS data and status switch data. The GPS data is 0 or 5 V level serial stream coming in on one line at 9600 baud. The status switch data comes in as 0 or 5 volt level signals into a latch on the flight computer. There are eight channels available on the latch.

3.4.2.3 Umbilical Communications

Umbilical communications consists of an RS-422 serial communications link between the flight computer and a PC in the block house. Umbilical communications is desired for pre-launch testing of the flight computer, data retrieval, and if necessary, for reprogramming the microcontroller. Four RS-422 lines are required through the umbilical plus one microcontroller flash programming control line.

3.4.2.4 Output to Transmitter

Output to the transmitter is a high speed, 0-1 V serial data stream through an SMA connected coaxial cable.

3.4.2.5 Power Connections

The flight computer requires power inputs of +5 V, +15 V, and –15 V. Table 3.4.2.2 details these connections and includes an estimated power budget. Figure 3.4.2.5 shows regulator schematics where the +/-15 V are down converted to –5 V, +/-6 V, and +12 V.

Table 3.4.2.2: Required Voltages and Power

Voltage	Estimated Power Consumption
+5 V	0.75 W
+15 V	0.7 W
-15 V	0.6 W

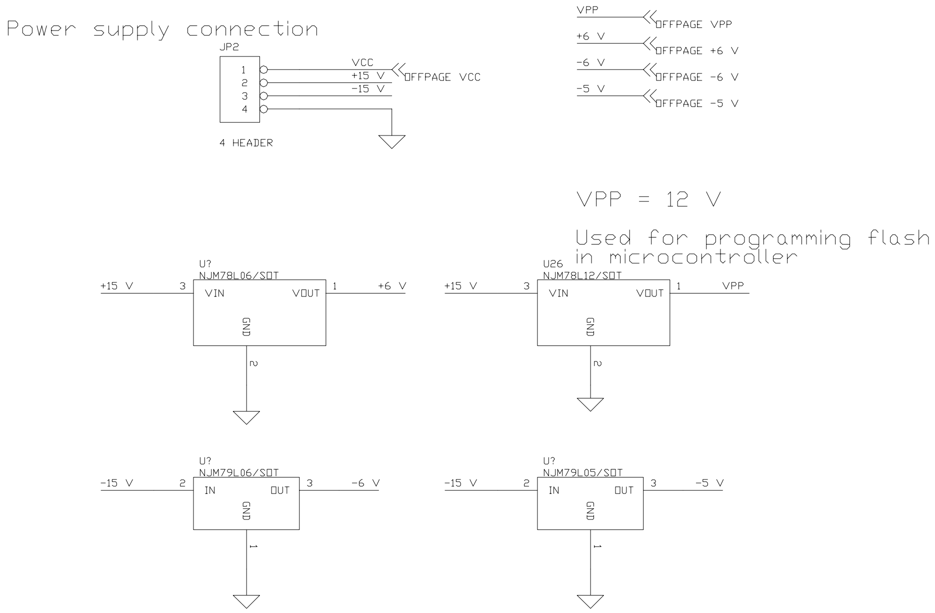

Figure 3.4.2.5: Voltage Regulators

3.4.3 Hardware

The following summarizes the major hardware components that are used in the flight computer.

3.4.3.1 MH68HC916Y1 Microcontroller (Figure 3.4.3.1)

The HC16 controller is the brains of the flight computer, controlling the timing of the ADCs, formatting all data into packets, and storing and transmitting those packets. It is a 16-bit device operating at 16.78 MHz with 48 kB of flash EEPROM and 2 kB of RAM.

3.4.3.2 CompactFlash Nonvolatile Memory Card (Figure 3.4.3.2)

The CompactFlash memory storage card is a popular memory card used in such products as PDA’s and digital cameras. It is available in sizes beginning at 4 MB to over 256 MB. With SRP-4’s expected data budget and flight time, it is expected 6 MB of storage space will be required. The CompactFlash requires 512 byte block transfers for each write cycle, thus the 512 byte packet format, as discussed in the software section.

3.4.3.3 ADS7815, ADS7820, and ADS7821 Analog-to-Digital Converters

The ADC’s are successive approximation converters with 250 microsecond sample-and-convert periods and 16-bit parallel output.

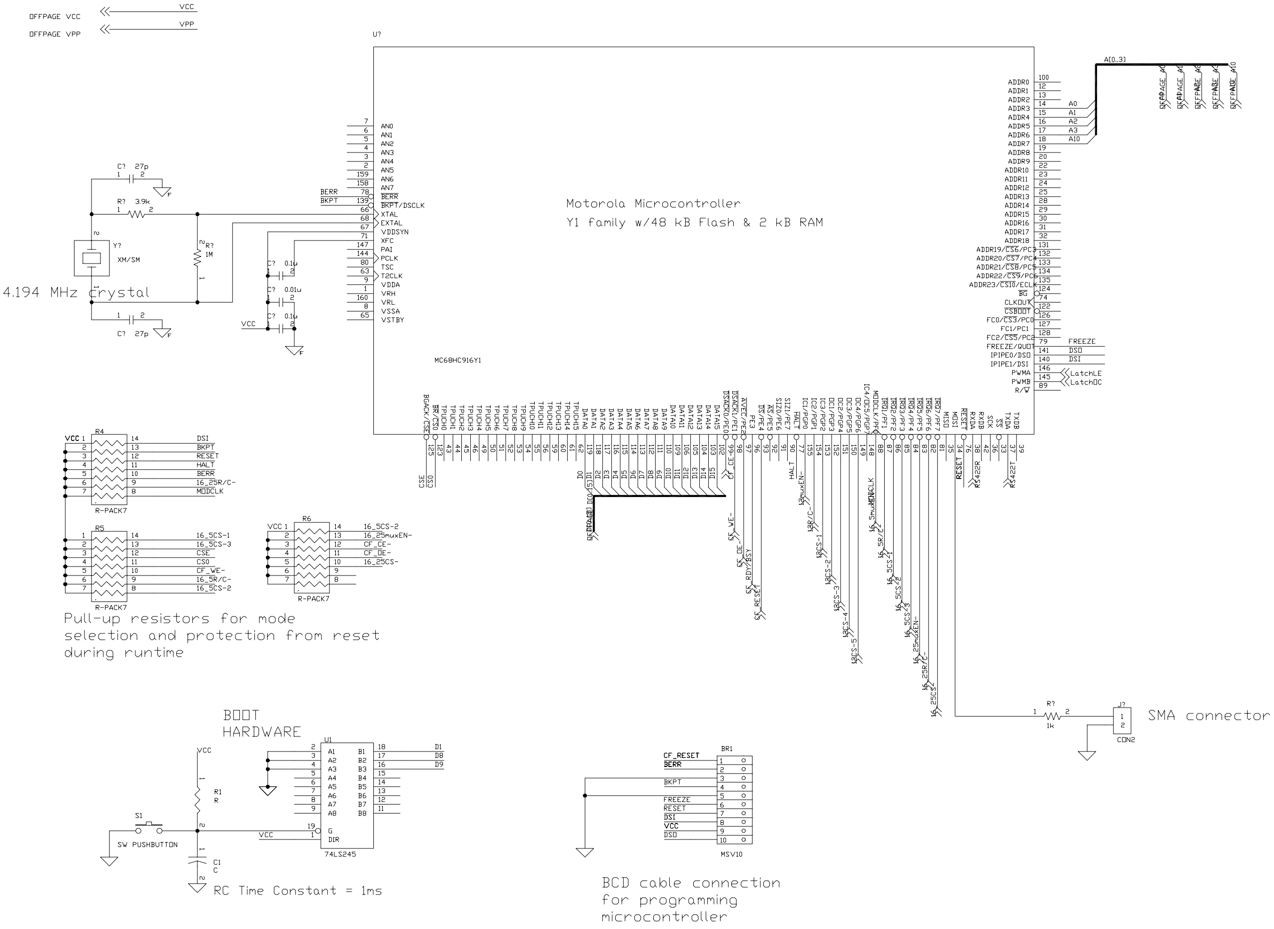

Figure 3.4.3.1: Microcontroller Schematic

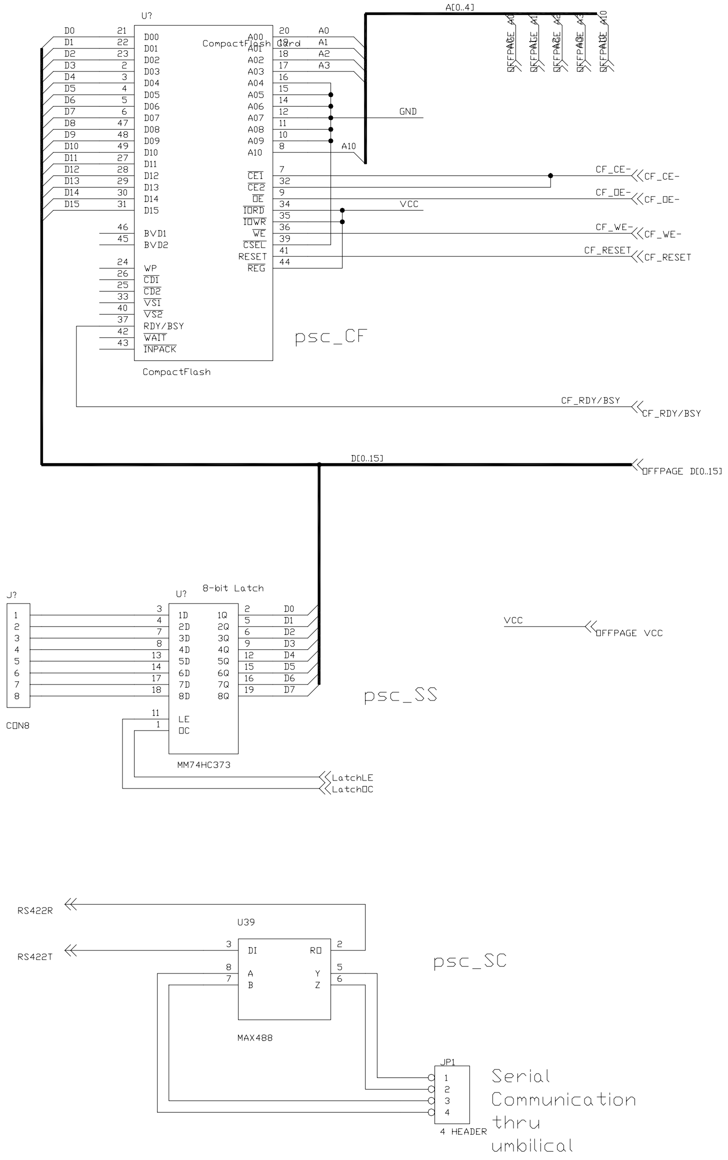

Figure 3.4.3.2: CompactFlash, Latch and Serial Communication Schematic

3.4.4 Flight Computer Software

Analog-to-Digital Conversion Loop

The analog-to-digital conversion loop is a 100 ms loop consisting of ten 10 ms loops. In each 10 ms loop five of the forty 12-bit channels are sampled once and all 16-bit channels are sampled once. Eight of the ten 10 ms loops sample five 12-bit channels, thus sampling all forty 12-bit channels at least once every 100 ms, or at a rate of 10 Hz. Since all 16-bit channels are sampled within each 10 ms loop, they get sampled at a rate of 100 Hz. This is illustrated in the flowchart in Figure 3.4.4.1.

There are possible timing problems which may arise. The signals from the multiplexers must have enough time to settle, so as not to sample signals that still contain transients. There are also additional delays associated in the conversion process. These problems can be found and eliminated through testing and do not pose a major threat.

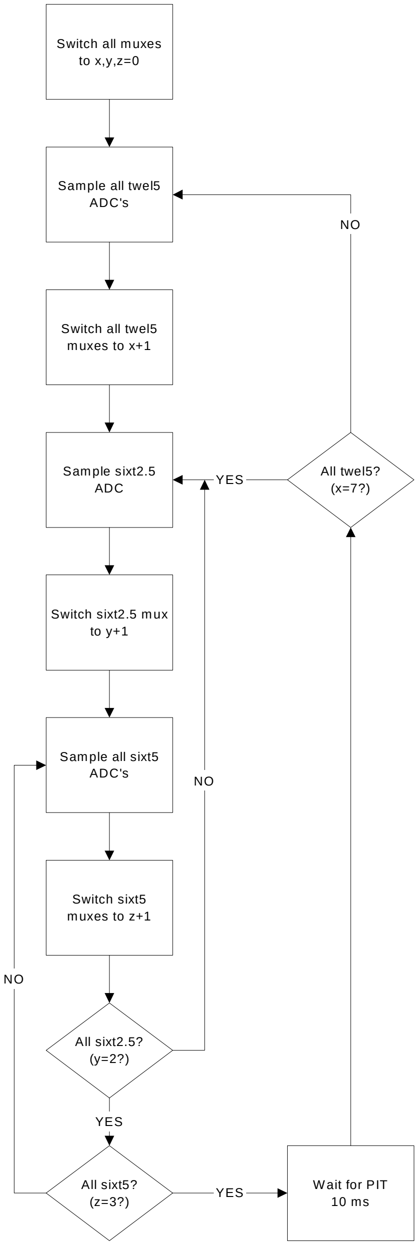

Figure 3.4.4.1: ADC Sampling Loop

Microcontroller Program

An overview of the microcontroller program is shown in Figure 3.4.4.2. The loop is designed to operate as follows

- On reset, the microcontroller will first determine if the vehicle has been launched. If launch has occurred then this reset was an unplanned reset in flight, and the best course of action is to return to collecting data as quickly as possible since no diagnostic and repair capability is available onboard. If launch has not occurred, the microcontroller will perform an onboard health check.
- The system will next begin to collect data, whether on the ground or in flight. This is the main loop for the microcontroller, and is an infinite loop.
- Packets will be constructed by combining the data from 10 iterations through this main loop, retrieving data from the 100Hz sensors each iteration, and from the 10Hz sensors on the first of the ten loops.
- Error detection codes will be constructed as data is read, and the packet will be stored in main memory (RAM).
- On iterations 2-9 of each 10 iterations through this loop, a check will be made to determine if there is a GPS data packet ready in the TPU. If so, the GPS data packet will be sent to the transmitter and to the flash memory. If not, the last data packet will be written to flash memory.
- On iteration 10 of each 10 iterations through this loop, the flight and science instrument data packet will be sent to the transmitter.
- After the work necessary for an iteration through the loop has been completed, the flight computer will wait for the periodic 10ms timer to expire before continuing to the next iteration. This timer will be implemented using the Periodic Interrupt Timer (PIT) in the Single-Chip Integration Module (SCIM) of the microcontroller. When this time expires, it generates an interrupt and starts counting down a new time interval. By using this method, we can ensure that the start of each instrument reading cycle occurs at consistent time intervals.
- Before returning to the start of the loop to read the next data sequence from the instruments, the watchdog timer will be reset. This timer will have a period of 25ms, so that if the flight computer software should not complete a sequence of readings and issue an interrupt from the PIT in the a time span that should have allowed for at least two reading cycles to occur, the flight computer will be reset.

It is likely that we will need to test the microcontroller functionality while the flight computer is integrated into the vehicle. To enable this, the flight computer will check for a test mode signal at reset, and if this signal is present all data packets will be sent across the serial connector in addition to the transmitter.

The correct operation of this algorithm is dependant on the possibility of several operations being competed within each 10ms iteration through the main loop. Since the flight computer hardware is not available at this time, we have been unable to verify that this requirement can be met. In the event that it cannot, the main loop would require a redesign to allow interleaved data packets to be sent without loss of data.

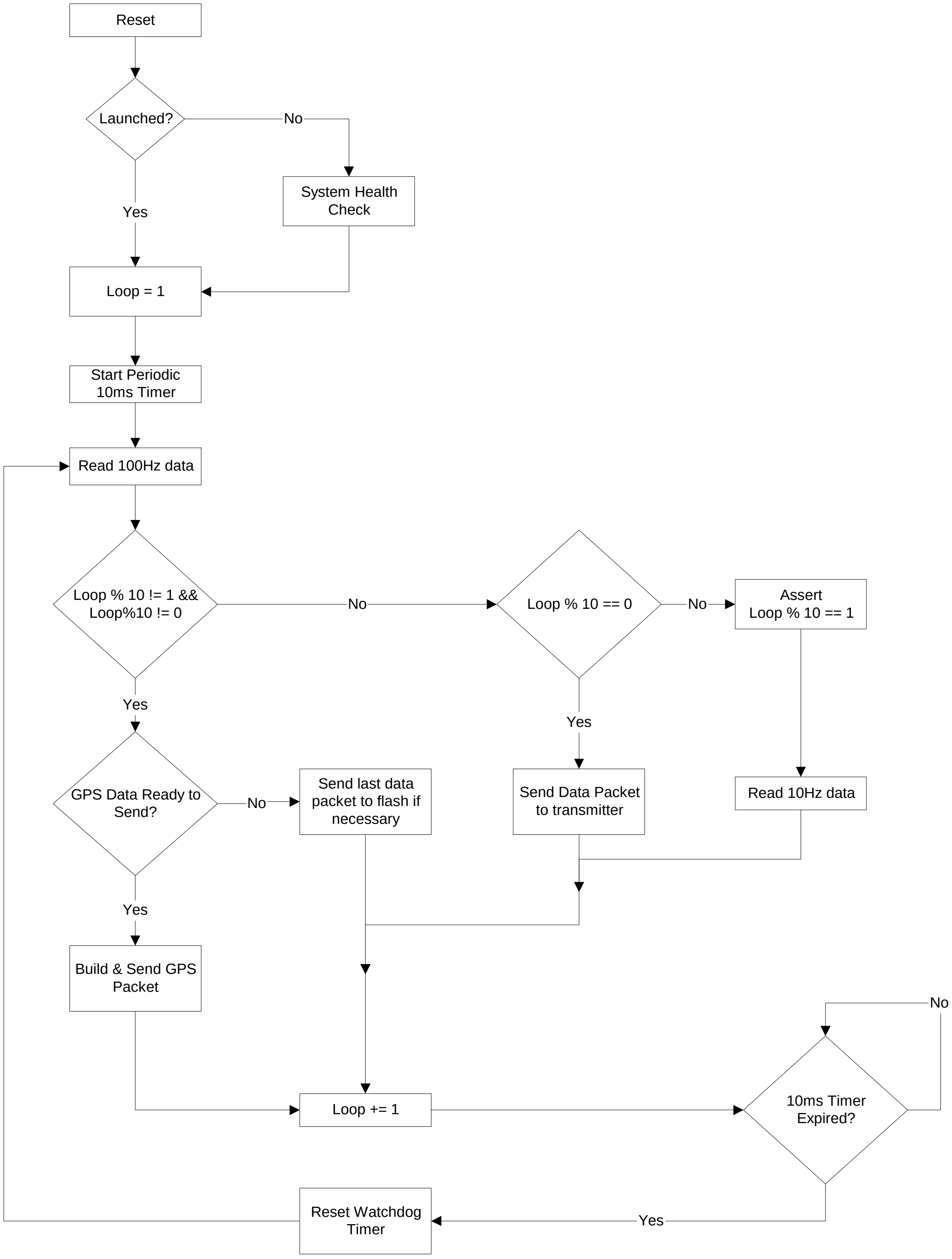

Figure 3.4.4.2: Flight Computer Software Flowchart

All data created by and input into the flight computer must be stored in NVM and transmitted to the ground station in a format that is decipherable. The same packet format was chosen for both NVM storage and transmission so that only one software package would be needed to read the data. Because storage of data in NVM requires blocks of 512 bytes be written in one write sequence, packets are to be 512 bytes in length. Two packet types will be handled by the flight computer. First, flight and science data will make up of one packet type that will include a unique sequence of 48 bits that identifies the packet type as flight and science data. The second packet type will be identified as GPS data by a different sequence of 48 bits. All packets will include the starting and identifying 48 bits (6 bytes), a time stamp, the data, the error checking parity data, and a sequence of stop bytes. Figure 3.4.4.3 illustrates the packet format, and the start and stop bytes.

Packet Format:

6 Start Bytes	Time Stamp	Flight, Science and GPS Data	Parity Bytes	6 Stop Bytes

Flight & Science Data Packet Start Bytes:

1	1	1	0	0	0	1	1	Pattern continued and repeated for total of 6 bytes

First Byte

GPS Data Packet Start Bytes:

1	0	1	0	1	0	1	0	Pattern continued and repeated for total of 6 bytes

First Byte

Stop Bytes for All Packets:

1	1	0	0	1	1	0	0	Pattern continued and repeated for total of 6 bytes

First Byte

Figure 3.4.4.3: Packet Format

3.4.5 Testing

Hardware Testing

It is critical that the clock signal be tested to ensure that sampling loops are as close as possible to 10 ms. An oscilloscope fast enough to measure 16 MHz signals accurately will be required. The main clock frequency and the Periodic Interrupt Timer are adjustable with software.

Care was taken in the design to minimize noise that is introduced by the flight computer onto the analog data signals. Testing will need to be done, and the design changed if necessary, to ascertain that the noise is as small as possible, ideally less than 38 microVolts.

Testing will need to be done after integration into the payload to make sure excessive noise is not introduced by other instruments. If that happens, then steps will need to be taken to minimize that noise.

The hardware will need to be temperature tested. Most parts are designed to withstand –45ºC to 85ºC, so the flight computer will need to be tested in that range.

After integration and before flight of the payload, the flight computer should be characterized for changes to signals due to noise introduced by the flight computer itself, by the surrounding instrumentation, and by temperature changes. The characterization will help those analyzing the retrieved data.

Software Testing

- It is imperative to the correct operation of this program that any operation to be undertaken during a single loop should be completed within 10ms. Testing to ensure that this occurs is critical.
- The error detection scheme should be implemented on a non-embedded system, and tested to determine its effectiveness in detecting errors. This should include testing for random bit errors, and also for the burst type errors that are common in this type of communication system.
- The software should be loaded onto the flight computer, and simulated inputs on each of the sensor lines should be created to ensure that the flight computer correctly detects and reports values throughout the input ranges.
- The sensors and GPS should be connected to the flight computer, and the sensors and GPS values should be accurately detected and reported by the flight computer.
- The umbilical should be connected to the flight computer in order to verify that the output across the umbilical connection correctly reflects the sensor and GPS readings.
- The transmitter should be connected to the flight computer, in order to test that the output via the transmitter correctly reflects the sensor and GPS readings.
- The flight computer should be reset during operation, to ensure that sensor and GPS readings continue correctly after the reset.
- The launch detect function of the flight computer should be tested.
- The contents of the flash memory should be tested, both a short while after a sequence of write operations, and after the flight computer module power has been removed and reconnected.
- The time stamping of each sequence of sensor readings should be checked to ensure it conforms to the 10ms period we require.

3.4.6 Future Enhancements

PC Software could be produced that provides an interface between user and microcontroller software. This would enable the user to configure the software for future missions without an in-depth knowledge of the code. This interface would only be valid for relatively similar missions, in that the basic setup of the flight computer would not change, although the instruments and data rates could be different.

The interface would allow the user to select the data rate for each input line, including disabling that data line. Data rates would be chosen from a list, probably including 10Hz, 50Hz, and 100Hz. The interface will modify on the code by manipulating #define values and functions in a header file, which will then be substituted into the code by the preprocessor during the code build process. The time length of the periodic timer would be set by assigning a value to PERIODIC_TIMER_LENGTH. The value will be the number of milliseconds required to read the fastest data rate. The value of LOOPS_PER_PACKET will be set based on the fastest data rate as follows:

- 100Hz, set to 10
- 50Hz, set to 5
- 10Hz, set to 1

A determination of whether the processor can read the required data within the time allotted will be made, and the user will be notified if the rate is too high. The functions *read100Hz*, *read50Hz*, and *read10Hz* in the file *ReadDataFuncs.c* will be modified to include the code necessary to read data from the input lines selected by the user. The code in this section will also be optimized so as to reduce the number of multiplexer selection operations. The main control loop of the flight computer program will be selected from three options based on the value of the LOOPS_PER_PACKET definition. The code will be recompiled using the new files. It will be the responsibility of the user to test that the recompiled software performs as expected.

3.5 Communications

General Requirement

The communication system will transfer data from the rocket to the ground support equipment via a telemetry link.

System Overview

The general block diagram of the communications system is illustrated in Figure 3.5.0.1 The house keeping and science instrumentation sensor signals are sent to analog conditioning circuitry before being fed into the flight computer. The flight computer digitizes and multiplexes the analog instrumentation data into a serial bit stream. The serial bit stream is forwarded to a telemetry transmitter that transmits the data to a ground station. The ground station receives, recovers, stores, and displays the data.

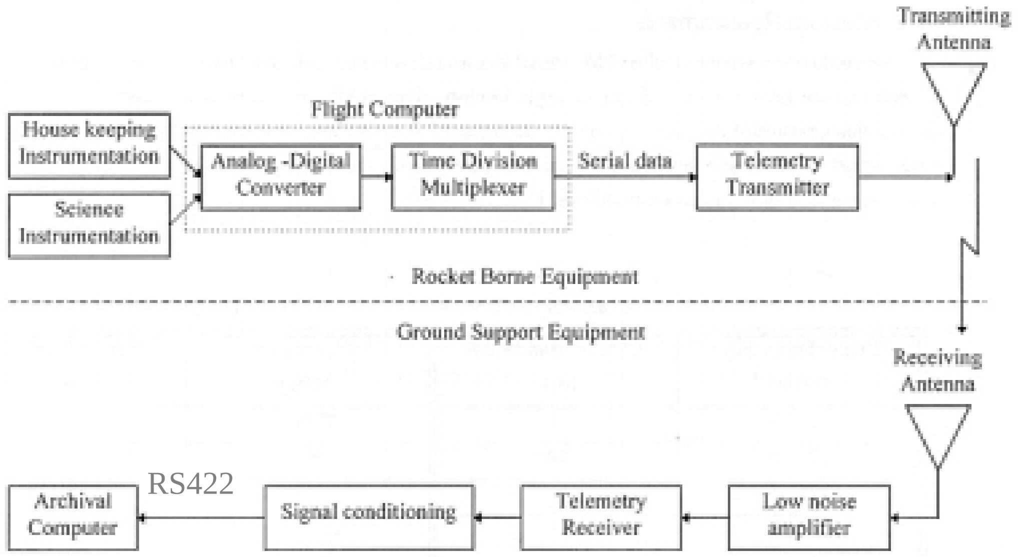

Figure 3.5.0.1: The general block diagram of the communications system

3.5.1 Transmitter

Functional Requirements

The transmitter must frequency modulate a input digital signal into S-band and output at least 2.5 Watts of power into a patch antenna.

Overview

The transmitter designed for SRP-4 was built by Stephen Bruss. S-Band transmitters are used because the Poker Flat Research Range (PFRR) supports S-Band equipment.

Electronic interface Requirements

- Carrier frequency Range: 2.2 – 2.3 GHz
- Frequency Stability: 0.001%, 10PPM
- Voltage 24-32 V DC
- Power output: 3 W
- Power consumption: 18 W at 28 V
- Current 50 mA (max) at 28 V
- Modulation: FM
- Deviation: +/- 8 MHz max
- Deviation linearity: 2.5% max. BSL for +/-8 MHz deviation
- Start up time: < 5 seconds
- Antenna compatibility: 10:1 VSWR
- Harmonic/spurious response: -40 dBc
- Input impedance: 220 Ω
- Input voltage: 1 V peak-peak
- Frequency response: 1 dB; 3 dB
- Presentable under-voltage and over-voltage RF system shutdown

Design Issues

According to Stephen Bruss's suggestion, 1 V p-p is a good input voltage level. Since the transmitter uses AC coupling, as long as the input level is limited in 1 V p-p, the voltage range inside the transmitter will be –0.5 V to +0.5 V. No voltage match circuitry is required.

Although the specification says the nominal impedance is 220 Ω, it is significant only for a high frequency input signal. In SRP-4, the data rate is approximately 40 kHz. Even if the impedances do not match, the reflection will not influence the input. Therefore, impedance match circuitry is not necessary here

Digital NRZ code is used. At the receiving end, the digital regenerator can recover the synchronous signal from NRZ code.

Because the modulating signal in SRP-4 is digital, the transmitter modulation linearity will not be a problem. The input digital signal bit rate will be no more than 300bps. For NRZ signals, the baseband bandwidth will be no more than 300kHz. In this range, the frequency response is flat regardless of the setup of the attenuators. The pulse width will be no less than 1/300 kHz = 3.3 us. According to Bruss, a 10ms long continuous DC signal will cause errors. This means when 3000 continuous 1s or 0s are transmitted, the DC response problem will be significant. However, 3000 continuous bits of the same value is so improbable that it can safely be ignored.

Data rate (hereafter, data rate means the total bit rate from the flight computer, including frame overhead and correction coding) is 40 kbps.

The center frequency of the transmitter (and consequently the whole system) is to be set to 2.2155 GHz. The frequency range of the transmitter is designed to be 2.2-2.3 GHz (with the stability of +/-22 kHz). This frequency range was chosen because it is a designated frequency for telemetry at Poker Flat. PFRR has four designated FM telemetry bands with 16 MHz bandwidth, and eight 3 MHz wide bands, as illustrated in Figure 3.5.2. The center frequency of the patch antenna was set to 2.2155 GHz, with a bandwidth of 16 MHz. Although SRP-4 has a relatively low data bit rate and 16 MHz is probably not necessary, to match the patch antenna a center frequency of 2.2155 GHz is chosen.

In the Mission Initiation Conference, NASA pointed out that there might be a conflict in the 2.2155GHz channel. Further investigation is required and it may be necessary to change to the 2.2355GHz channel. Then the patch antenna would have to be re-designed.

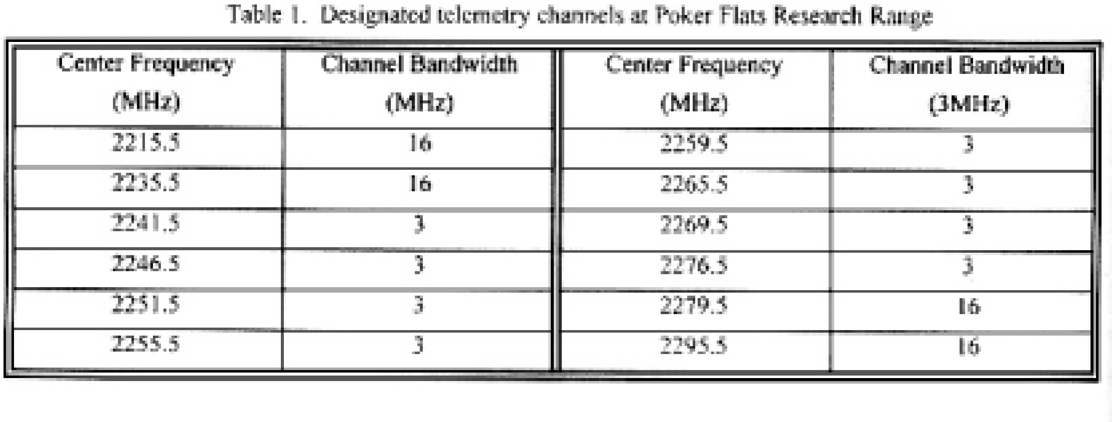

Table 1. Designated telemetry channels at Poker Flats Research Range

Center Frequency (MHz)	Channel Bandwidth (MHz)	Center Frequency (MHz)	Channel Bandwidth (3MHz)
2215.5	16	2259.5	3
2235.5	16	2265.5	3
2241.5	3	2269.5	3
2246.5	3	2276.5	3
2251.5	3	2279.5	16
2255.5	3	2295.5	16

Table 3.5.1.1 Designated telemetry channels at Poker Flats Research Range

The frequency deviation is set at 300 kHz. In FM modulation, if the modulating signal band has the maximum frequency of $f_{\max}$, and the maximum frequency deviation of the modulator is Δf, the bandwidth of the RF signal can be estimated by Carson's rule:

$$B = 2 \cdot \left(\Delta f + f_{\max}\right)$$

Where $B, \Delta f, f_{\max}$ are all in Hz.

In order to reduce the noise at the receiver input, the minimum bandwidth is expected. On the other hand, wider bandwidth is also desired to achieve more FM improvement. Compromising the receiver noise bandwidth and FM improvement, the spectrum at the transmitter RF output is illustrated in Figure 3.5.1.1

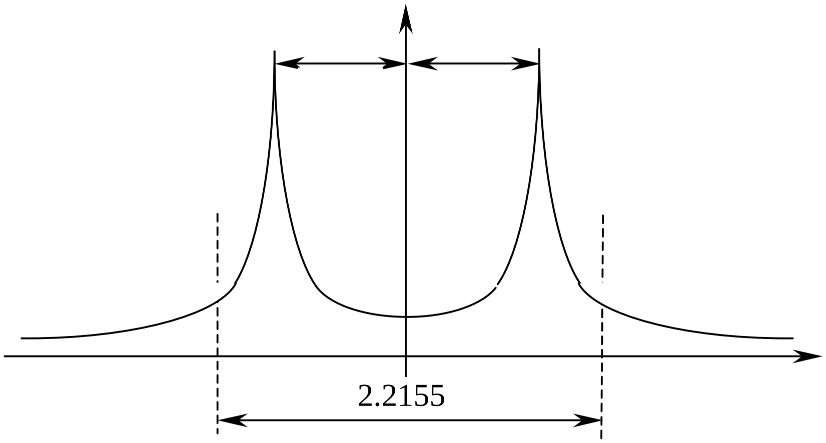

Figure 3.5.1.1: The spectrum at the transmitter RF output

Doppler Shift: If the vehicle moves away from the observer at 700 m/sec, then the Doppler shift for a 2.2155 GHz carrier is calculated by the Doppler Shift Formula

$$\Delta f = \frac{f \cdot v}{c}$$

where v is the velocity of the rocket and f is the carrier frequency in Hz, and c is the speed of light in m/s. It turns out to be 5 kHz. For narrow band signals, it could be a significant influence. For SRP4 however, FM will spread out the spectrum so doppler shift is negligible.

Set-up Procedure

The DB9 port built on the transmitter is used to supply DC power and set up transmitter parameters. Pin 1 and pin 5 connect to 28 VDC. Pin 2 is data output referring to the transmitter, and pin 4 is data input referring to the transmitter. Pin 6 to pin 9 are all ground. The other end of the data cable is the RS 232c serial port on an ordinary PC. However, a converter is required to match the physical feature of the transmitter data port (0, +5 V CMOS) and RS 232c (-10, +10 V). After wiring-up, a Transmitter Interface Program written by Stephen Bruss has to be installed on the PC connected to the Transmitter. The source code is provided in his thesis. After starting the program port base address, interrupt vector number, IRQ and baud rate parameters are shown. Set up the proper interface on the PC if necessary. In Bruss's thesis (P.58), a brief manual of the usage of the program is introduced. Here is recommended configuration and the explanation if not mentioned in previous subsections. The configuration values are stored in the EEPROM of the system controller.

- RF Frequency: 2215500000 (Hz)
- Attenuator 1: 200 (estimated)
- Attenuator 2: 200 (estimated)
- RF Oscillator: on
- Med Power Amp: on
- High Power Amp: on
- Frequency lock: Locked
- TCXO Correction: 50 TCXO Loop: closed
- Low Volt Dropout: 0

- Low Volt Restart: 0
- High Volt Dropout:
- High Volt Restart:
- Voltage Dropouts: disabled

When TCXO (Temperature Controlled Crystal Oscillator) correction is set closed, TCXO will work automatically.

There are two stages of attenuators used to control the maximum frequency deviation. The transmitter has a fixed FM frequency deviation to input voltage ratio, r, in Hz/V. The attenuator output voltage is t multiplied by input voltage, where t is the attenuator ratio determined by the attenuator set-up. So if the input has a V p-p voltage level, the maximum input voltage deviation is V/2, the maximum frequency deviation will be set as:

$$\Delta f = \frac{V}{2} \cdot r \cdot t$$

Use a spectrum analyzer to check the output 3-dB bandwidth. Empirically set it to 300 KHz. To set the attenuators for minimum noise, set the first attenuator to the least attenuation and the second to the most. The opposite is true for distortion. So making the two values close is recommended.

Assembly notes

- Temperature: -30 °C to +50 °C base plate
- Vibration: about 2000 Hz of deviation per G
- Altitude: unlimited
- Humidity: 85% Relative Humidity
- Dimensions: 2.00” x 5.00” x 1.94” +/- 0.050”
- Weight: 440 g +/- 25 g
- Connectors:
  - RF out: SMA
  - FM modulating input: SMA
  - Power and system controller interface: DB9 male

Testing

- Set the attenuators
- Attach the transmitter to 28 V 2 A power supply
- Attach the power and/or spectrum analyzer to the transmitter output
- Connect the transmitter data input to ground
- Measure the output power and the center frequency
- Connect the transmitter data input to a signal generator. The output signal is square wave NRZ pseudo-random digital signal with a bit rate of 35 Kbps. The signal has 1 V peak-to-peak amplitude.
- Measure the output power, center frequency and the bandwidth.
- Expected value: center frequency, 2.2155 GHz; output power, 2.5 W; bandwidth, 300 KHz

3.5.2 Patch Antenna

Functional Requirements

Power rating > 2.5 W, omni-directional, gain > -10 dB

Interface Requirements

A 4-way splitter is required to connect the transmitter and the patch antenna. (Mini-Circuits ZB4PD-42, 1700-4200 MHz, www.minicircuits.com). All connectors are SMA, 50 Ω.

Design

The transmitting antenna on the rocket is a microstrip patch antenna, designed and built by Ty Sullins. It is omni-directional and circularly polarized, with a central frequency of 2.2155 GHz and a bandwidth of 20 MHz. It has a theoretical gain of 0 dB.

In previous ASRP missions, the antenna on the rocket has been linearly polarized and the ground station antenna has been circularly polarized. The circularly polarized ground station antenna ensured that the telemetry signal was received despite the orientation of the linearly polarized antenna on the sounding rocket. However, the polarization mismatch between the linear and circularly polarized antennas results in a 3-dB loss. Ty Sullins designed a circularly polarized sounding rocket antenna, which overcomes the 3 dB mismatch loss of the linear polarized antenna.

The microstrip antenna is lightweight, thin, conformal, and inexpensive to fabricate. Circularly polarized waves can be generated using simple geometries. The main limitation of microstrip antennas is their narrow bandwidth.

The antenna is already fabricated. It is composed of four identical pieces with four patches on each piece, for a total of 16 pieces. Power from the transmitter goes through a four-way power splitter to each of the pieces. Each branch will be in turn fed into four patches. At each port, 50-ohm SMA connectors are used.

One issue of concern is the reduced antenna gain when the rocket is at high altitudes and the communication path has a very sharp angle to the surface of the antenna. The radiation pattern of the patch antenna as a whole is theoretically spherical. The test result of radiation pattern is illustrated as Figure 3.5.2.1. The largest loss will be about 3 dB, which is within the acceptable maximum antenna gain –10 dB.

Assembly Notes

Mounting holes, SMA connector holes need to be drilled on payload tube. A drilling template will be provided to the mechanical team. To minimize coax cable losses, the coax cable should be as short as possible. The antenna should be located so that a protective shield is not necessary. Shield will introduce losses. The specifications of the power splitter can be found at www.minicircuits.com (12/20/2000).

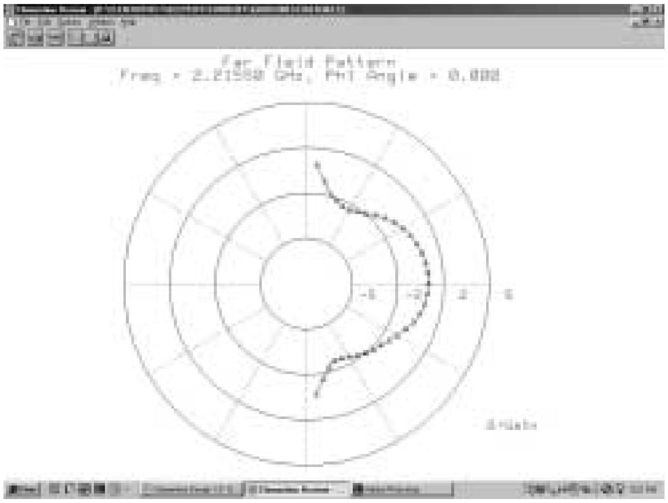

Figure 3.5.2.1: The radiation pattern of the patch antenna

3.5.3 Dish Antenna

Functional Requirements

The antenna and the feed receive the power transmitted by the patch antenna. During rocket flight, the antenna should be pointed for maximum power reception.

Interface Requirements

Interface: SMA, 50ohm output.

Design

The ground-receiving antenna uses the same scheme as before. The antenna dish and the feed are all built. The main issue is pointing the antenna toward the rocket.

To obtain the position of the rocket, radar data will be collected at the control house. The radar data then will be converted into pointing data (i.e. azimuth and elevation angles), which will be vocally transferred from the control house to the operator standing at the dish through a walky-talky. The operator will manually adjust the pointing angles to keep in track with the rocket.

The feed will be mounted at the point of dish focus, which is on the pole crossing the dish. The feed will face back to the dish. What was done before was facing the feed directly to the rocket at the beginning of launching and flipping the feed over when the rocket is far. It is feasible due to the fast movement of the rocket at launching time and the wider beam width of the feed itself. It was successful but not necessary. The dish has a diameter of 1.22 meter. The launching stand is 1 mile away from the dish. According to equations

$$\boldsymbol{\theta = \frac{1.2\lambda}{D}},\ \boldsymbol{w = 2 \cdot r} \cdot \sin\left(\boldsymbol{\frac{\theta}{2}}\right)$$

θ is 0.133 radian (7.6°) and the cross-section of the beam will have a diameter w of 0.132 miles. So there will be enough time to manually point the antenna toward the rocket. The distance from the rocket to the station was close enough so the carrier to noise ratio threshold was met.

The analysis above also shows that an automatic pointing tripod is not necessary. The tripod, the mounting material for the dish and feed, the counterweight to balance the dish and make it easy to manipulate, and the meters to read the pointing angles have all been made (SRP-2).

Assembly Notes

Coax cables and LNA should be chosen to minimize losses between antenna feed point and receiver. The loss must be no more than 20 dB or else the link budget fade margin will be exceeded.

3.5.4 Low Noise Amplifier

Functional Requirements

The low noise amplifier (LNA) pre-amplifies the received signal and reduces the system noise. The frequency range of the LNA should cover the signal frequency range. The gain of the LNA should be at least 20 dB. The cable loss from LNA to the receiver is not exactly known, but it is estimated to be as high as 20dB. If the actual loss is greater than 20 dB, a higher gain LNA might be necessary.

Interface Requirements

The LNA has a SMA 50 Ω input and requires 70 mA at 15 V. It must run for a minimum of 1 hour, but for planning purposes, a minimum of 1-½ hours will be assumed. Either a battery or DC power supply is required. The LNA will be quite a distance from available power (for the DC power supply) so a battery (if one is available) would be the best choice. The battery must provide 15V and 105 mAh.

LNA Specifications

A Mini-Circuits ZEL-1724LN low noise amplifier will be used. More specifications can be found at www.minicircuits.com (12/20/2000). As mentioned in the Functional Requirements section, if a higher gain LNA is needed, the Mini-Circuits ZHL-1724VLN (28 dB gain) and ZHL-1724HLN (30 dB gain) should be considered. However, both of these LNAs have high power consumption. So power supply plan will have to be changed, too.

ZEL-1724LN								
Frequency MHz	GAIN, dB		Maximum Power, dBm		Dynamic Range		DC Power	
f_l - f_u	Min.	Max. Flatness	Min.	Input (no damage)	NF dB Typ.	IP3 dBm Typ.	Cur-rent (mA)	Volt(V.)
1700-2400	20	±1.00	10	13	1.5	22	70	15
L =low range(f to f /2) U=upper range(f /2 to f)								

Table 3.5.4.1: The specifications of the selected LNA

Power supply

Energizer provides a battery in their Eveready line that provides 15 V and 140 mAh. This would power the LNA for approximately 2 hours, which is more than enough time. The battery is available from Newark and cost and other information is given below. The two batteries will be connected parallel in order to back up each other as well as provide long life. These batteries will need to be cold weather tested since they will be outside in March weather.

Stock #	Model	Vendor	Description	Web Site	Price per	Quantity	Total Price
03F7084	411	Energizer	15V,140mAh battery to power LNA	www.newark.com	$ 7.28	2	$ 14.56

Table 3.5.4.2: The specifications of the selected LNA battery

Assembly Notes

The coax cables and LNA should be chosen to minimize losses between the antenna feed point and receiver. The dimension and other assembly specifications can be found at www.minicircuits.com. The dimension and other assembly specifications for the battery can be found at www.Newark.com. The power line from battery to the LNA should be made. A small circuit for LNA power connection is required.

3.5.5 Receiver

Requirements

The receiver must demodulate the received signal back into base band. The bandwidth should be set to maximize the signal to noise ratio, S/N.

Interfaces

A 120VAC power outlet is needed. The coax cable from the LNA to the receiver should be at least 75 ft long. The connectors are SMA at the LNA end and N-type at the receiver end. The connector to the digital regenerator is a N-type connector.

Design

The receiver that will be used is a Microdyne telemetry receiver model 1400-MRA. The RF Tuner plug in module is a 1415-VT 2200-2300 MHz model. The IF Filter Amplifier plug in module is 1420-I series model. The Demodulator plug in module is 1458-D multi-mode demodulator.

RF input signals are applied to the receiver via the rear panel connector “RF INPUT”. Demodulated signals are extracted from rear panel connector “VIDEO OUT 1”. Here “VIDEO” does not necessarily mean video signal, but general output signal. On the rear panel, in the “VIDEO” region, set “MODE FM/PM” to “FM”, and set “COUPLE” to “DC”.

RF Frequency	2215.5 MHz
IF Bandwidth	3300 kHz
Video Bandwidth	50 KHz
Modulation FM	
Video Gain 44 or output voltage close to 1 V p-p	
Loop Bandwidth	3 Hz
AGC Time Constant	0.1 ms
AFC Time Constant	1 Hz
2nd LO Mode	VFO

Assembly Notes

Coax cables and LNA should be chosen to minimize losses between antenna feed point and receiver.

Testing

- Connect the tested transmitter to the pseudo-random signal generator
- Shield the transmitter system with metal case.
- Use long cable to separate the transmitter and the receiver in order to reduce the effects of radiation leakage.
- Insert numerous attenuators between the transmitter and a power meter, use the power meter to measure the output power, adjust the attenuators to make the output power to –92 dBm.
- Take off the power meter.
- Connect the LNA to the attenuators, power up the LNA.
- Connect the receiver to the LNA, power up the receiver.
- Connect an oscilloscope to the receiver output.
- Verify the waveform at the receiver output. The output should have a data rate of 35 KHz
- Change the attenuation inserted and check performance

3.5.6 Digital Regenerator

Overview

The digital regenerator circuit was designed to perform two functions: re-timing of the received signal and the extraction of a clock signal from the received signal. Both functions can be achieved using a chip manufactured by Vectron International.

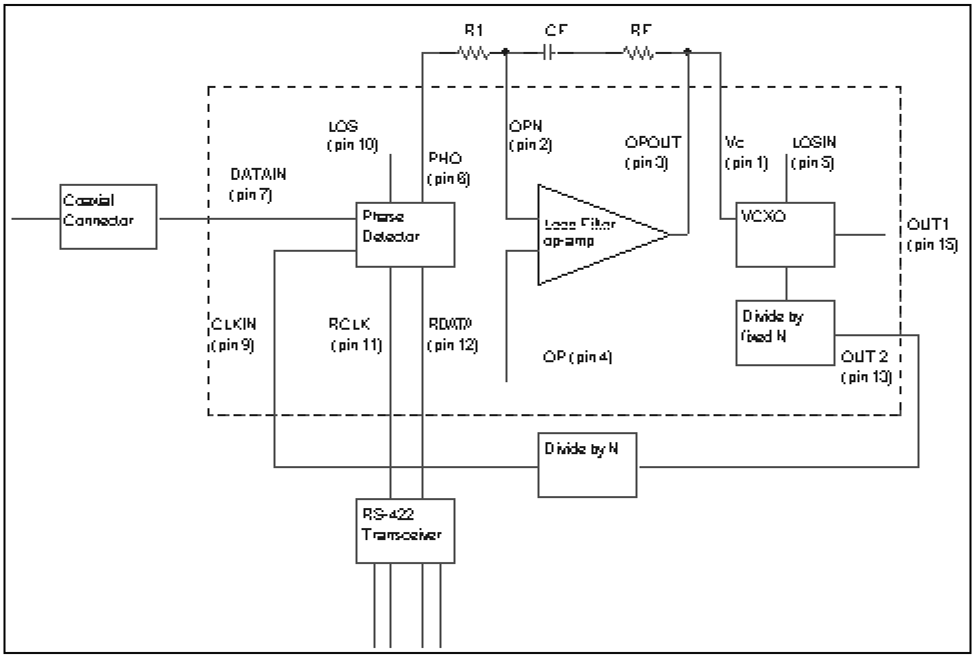

Figure 3.5.6.1: Circuit scematic of digital regenerator circuit

Design

The circuit schematic for the digital regenerator can be seen in the figure above. There are three main chips used in this design. They are the TRU-050 from Vectron (contains everything in the dashed line), an adjustable Divide by N (1-256) chip, and an RS422 transceiver.

The TRU-050 was designed to re-time data signals and extract clock signals at data rates as low as 8 kHz or as fast as 65.536 MHz. The chip contains four different sections which are a phase detector, loop filter op amp, VCXO, and a fixed 2^n divider. The phase detector is used in conjunction with a clock signal that equals the data rate for NRZ coding or is twice the data rate for RZ and Manchester coding. This clock signal allows the chip to synchronize with the incoming data. If the chip is not synchronized with the incoming data the digital regenerator will not work properly. The internal VCXO and the 2^n divider (where n can be selected from 1 to 8 at the time of ordering) can be used as the clock signal for the phase detector to synchronize with the incoming data signal or an external source can be used. The last component, the loop filter op amp, can be used to provide closed loop gain and bandpass filtering by attaching external resistors and capacitors. A program is available from Vectron's website (www.vectron.com 12/18/ 2000) can be used to calculate the appropriate values for the resistors and capacitors.

Many different frequencies and 2^n divider options are available. The one that seems to be the most flexible for this as well as possible future missions would be the TRU050-GECGA 32.1. This part number represent a chip with an VCXO of 32 MHz and a divider of 32, which results in a secondary frequency output of 1 MHz. An external divide by n chip could be connected to either the VCXO output (OUT1) or the 2^n divider output (OUT2) to provide a wide range of data rates. This would provide frequencies of 32 MHz or 1MHz , which ever was connected to, divided by any number from 1 to 256.

For a data rate of 40 kbs and NRZ coding the values in table 3.5.6.1 should be used.

Component	NRZ Coding
R1	7.08kΩ
CF	.01µF
RF	457kΩ
N	25

Table 3.5.6.1: Digital Re-generator set-up values

This chip has a loss of signal (LOS) pin. This output pin can be used to detect when the signal has been lost. The chip considers the signal lost if no transactions occur in any 256 consecutive clock signals.

For the RS422 transceiver the MAX488 can be used.

Interfaces

This circuit will require four interfaces including power (+5 volts), ground, a connection to the Microdyne receiver through a BNC, and a connection to the archive computer via RS422 connection.

Testing

There are several tests that can be preformed to see how well the digital regenerator performs. The digital regenerator should be tested to see how much the incoming data signal can be distorted and how well it cleans the signal up. It should also be tested to see how quickly it can lock onto the data frequency and over what range it can track the frequency if it drifts.

To perform the testing a frequency generator can be connected to the input of the digital regenerator and an oscilloscope can be connected to pin 11 and pin 12 (one at a time- pin 11 for recovered clock and pin 12 for recovered data) to see the output of the digital regenerator before it converted to RS422 protocol. The frequency generator can then be swept in the range of the desired data rate (40 kHz) to determine the circuits capture and lock ranges. For further testing the input can be distorted to see how well the digital regenerator can retime the data signal.

Cost

The cost of the digital regenerator circuit runs about $80.00. This breaks down as $50.00 for the chip from Vectron, $20.00 for the adjustable divide by n chip, and $10.00 for the circuit board, resistors, capacitors, and connectors that are needed.

3.5.7 Link Budget

The following list defines all the input variables used in the link budget

Rocket-Borne Transmitting System:

$f := 2.2155 \cdot 10^9$	Selected center frequency (designated frequency at poker flats).
$Strans_T := 34$ dBm	Output power of transmitter.
$Loss_T := 1$ dB	Losses due to cable attenuation and impedance mismatching from output of transmitter to antenna.
$GA_T := -10$ dB	Minimum gain of transmitting antenna for most of antenna coverage
$DR := 40 \cdot 10^3$ bits/sec	Data rate.
$f_{max} := 40 \cdot 10^3$ Hz	Baseband signal bandwidth
$\Delta f := 100 \cdot 10^3$ Hz	FM maximum frequency deviation

Ground-Based Receiving Station:

$diam := 1.22$ meters	Dish diameter in meters
$K := 0.55$	Aperture efficiency.
$Loss1_R := 1.0$ dB	Estimated Losses due to cable attenuation and impedance mismatching from output of antenna to low noise amplifier.
$Loss2_R := 20.0$ dB	Estimated Losses due to cable attenuation and impedance mismatching from output of low noise amplifier to front end of receiver.
$G_{LNA} := 20$ dB	Gain of low noise amplifier. (Mini-Circuits ZEL-1724LN)
$F_{LNA} := 1.5$ dB	Low noise amplifier noise figure. (Mini-Circuits ZEL-1724LN)
$B_{IF} := 300 \cdot 10^3$ Hz	IF filter bandwidth.(Set up by 1420-I IF Filter Amplifier Moduel on Mocrodyne 1400-MRA receiver.)
$F_{rec} := 12$ dB	Receiver noise figure. (Microdyne 1400-MRA)
$\gamma_b := 5$ dB	Minimum carrier_to_ratio for the receiver to detect the signal. Theoretical value is 0.

Enroute:

$Dist := 95000$ meters	Maximum distance between the rocket and the receiving antenna.
$L_{Atmos} := 1$ dB	Estimated atmospheric absorption loss.
$L_{Circ} := 1$ dB	Loss due to polarization. Both the transmitting patch antenna and the receiving dish antenna are circular polarized.

Miscellaneous constants:

$v := 3.0 \cdot 10^{8}$ m/s	Velocity of propagation through free space.
$k := 1.38 \cdot 10^{-23}$ J/K	Boltzman's constant
$To := 290$ K	Defined room temperature.

Link Calculations

Step 1: Find signal power transmitted from rocket.

Transmitted power from rocket $S_T := \mathrm{Strans}_T - \mathrm{Loss}_T$ $S_T = 33.0$ dBm

Step 2: Find power at receiving antenna flange.

Free space wavelength $\lambda := \frac{v}{f}$ $\lambda = 0.135$ meters/wavelength

Gain of receiving antenna. $GA_R := 10 \cdot \log\left[K \cdot \left(\frac{\pi \cdot \mathrm{diam}}{\lambda}\right)^2\right]$ $GA_R = 26.4$ dB

Free space loss from rocket to ground station. $fsL := 10 \cdot \log\left[\left(\frac{4 \cdot \pi \cdot \mathrm{Dist}}{\lambda}\right)^2\right]$ $fsL = 138.906$ dB

$$SF_R := \left(S_T - fsL + GA_T + GA_R\right) - L_{Atmos} - L_{Circ}$$

Power at receiving antenna flange. $SF_R = -91.465$ dBm

Step 3: Find effective noise power spectral density at antenna flange and calculate Fade Margin

Noise temperature of losses from antenna to LNA. $T_{Loss1} := To \cdot \left(10^{\frac{Loss1_R}{10}} - 1\right)$ $T_{Loss1} = 75.088$ K

Noise temperature of low noise amplifier. $T_{LNA} := To \cdot \left(10^{\frac{F_{LNA}}{10}} - 1\right)$ $T_{LNA} = 119.636$ K

3.5.8 Testing

Description

Connect the system following the complete communications system block diagram. Because the distance between the transmitting and receiving system is much closer than the actual situation, attenuators are required. The entire communications system must achieve the bit error rate of 10^{-7} and must work well within the fade margin.

Procedure

- Choose open outdoor test ground, avoid reflection
- Attach the tested transmitter to 28V 2A power supply
- Connect the transmitter to the pseudo-random signal generator. Shield the transmitter system with metal case
- Connect the four-way power-splitter and the patch antenna
- Insert enough attenuators between the transmitter and a power-splitter
- Setup the receiving subsystem
- Use the power meter to measure the output power after the dish antenna, adjust the attenuators to make the output power to –92dBm
- Take off the power meter
- Connect the LNA to the dish antenna, power up the LNA
- Connect the receiver to the LNA, digital regenerator to the receiver
- Attach a spectrum analyzer to the system output
- Measure the central frequency and the bandwidth.
- Connect a signal analyzer to the system output
- Check the waveform. It should be 35KHz NRZ square wave.
- Connect a computer running a data analyzer program based on the same pseudo-random number generator as the transmitter input.
- Measure the Bit Error Rate using the computer.
- The BER should be less than 10^{-7}.
- Change the attenuation inserted.
- Check performances, check the fade margin.

3.5.9 Pre-launch configuration

Dish antenna

- Ship the dish antenna to the specified spot.
- Mount antenna and bolt down, put the antenna dish on the tripod, put on the counterweight.
- Calibrate the pointing meters (azimuth and elevation).
- Mount the feed on the dish.
- Mount LNA on the tripod.
- Mound the battery for LNA then connect the LNA and the battery.
- Attach cables.

Receiver Station

- A seventy-five feet long cable is required to connect the LNA to the receiver in the station.
- Connect the digital re-generator and the archival computer

- Attach serial cables
- Power up Receiver
- Calibrate the receiver
- Set receive frequency to 2.2155 GHz
- Set video BW to 50 kHz
- Set IF filter to 300 kHz
- Set video gain to adjust the output voltage to 0.8 to 1 V p-p
- Power up serial board
- Power up archival computer
- Run archival compute

Communication initiation

- Power up the payload
- Double-check the synchronization and performance of the communication system
- Verify good data
- Voltage is as expected
- Other values are nominal